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ABSTRACT OF THE DISCLOSURE

Each of memory bridges and I/O bridges, cross-linked to one another, is provided with an interface circuit section which performs data transmission and reception according to an PCI-Express interface. Each interface circuit section has a communication error processing

5   section. When an error occurs in data received from the I/O bridge, the communication error processing section of the memory bridge cancels the received data and sends a communication error signal to the memory bridge. When receiving the communication error signal, the memory bridge stops receiving the data. Then, the communication error processing section of the memory bridge requests the I/O bridge to resend data.